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09/830,949	07/06/2001	Naohiro Hirose	250602US40PCT	5351

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EXAMINER	
CHAMBLISS, ALONZO	
ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
08/06/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	09/830,949	HIROSE, NAOHIRO	
	Examiner	Art Unit	
	Alonzo Chambliss	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 90-142* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 90-142* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/7/10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/7/10 has been entered.

Response to Arguments

2. Applicant's arguments filed 6/7/10 have been fully considered but they are not persuasive. In regards to Yabushita failing to disclose a lower level interlayer resin insulating layer and a lower via hole formed in the lover level interlayer resin insulating layer and the pad structure formed over the lower level interlayer resin layer. This argument is deemed unpersuasive because Yabushita discloses a lower level interlayer resin insulating layer 1 (i.e. a multilayered part of the substrate). A lower via hole (i.e. located at wiring 7) formed in the lower level interlayer resin insulating layer 1. An outermost interlayer resin insulating layer 6 formed over the lower level interlayer resin insulating layer 1. A pad structure 2 having an outermost conductor portion formed on the outermost interlayer resin insulating layer 6 (see abstract and Fig. 1).

In regards to Yabushita failing to disclose the planar area of the pad structure is greater than the planar area of the conductive circuit. This argument is deemed

unpersuasive because applicant has not disclosed the larger pad structure solves any stated problem or is for any particular purpose. Moreover, it appears that the pad structure of Yabushita when utilized in applicant's invention, would perform equally well with the different size pad structure. Therefore, it would have been an obvious matter of design choice to have wafers having different diameters, since such a modification would have involved a mere change in the size of a component. A change is size is generally recognized as being within the level of ordinary skill in the art. *In re Rose, 105 USPQ 237 (CCPA 1955).*

Specification

3. The disclosure is objected to because of the following informalities: fails to recite **the planar area of the pad structure is greater than the planar area of the conductive circuit**.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 141 and 142 recites the limitation " the core substrate" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1, 90-95, 98-109, 112-115, 117, 118, 120, 121, 124-127, 130, 131, and 133-142 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yabushita et al. (JP 08-172273).

With respect to Claims 1, 103, and 124, Yabushita discloses a lower level interlayer resin insulating layer 1 (i.e. a multilayered part of the substrate). A lower via hole (i.e. located at wiring 7) formed in the lower level interlayer resin insulating layer 1. An outermost interlayer resin insulating layer 6 formed over the lower level interlayer resin insulating layer 1. A pad structure 2 having an outermost conductor portion formed on the outermost interlayer resin insulating layer 6. A solder resist 5 (i.e. insulating cover coating layer) formed on the outermost interlayer resin insulating layer 6 and the pad structure 2. The solder resist 5 having an opening exposing a partially

exposed portion of the pad structure 2. A conductive connecting pin 3 (i.e. conductive connecting means) configured to establish an electrical connection with another substrate (i.e. modular substrate). The conductive pin 3 being secured to the partially exposed portion of the pad structure 2 via a solder 8. The solder 8 being disposed over the partially exposed portion of the pad structure 2, wherein the outermost conductor portion and the via hole 9 comprise an film 28 and additional film 21 from Fig. 8 formed on the film 28. A via hole 9 formed through the outermost interlayer resin insulating layer 6 and configured to electrically connect the pad structure to at least one conductive circuit formed below the outermost interlayer resin insulating layer, the via hole being positioned directly below the pad. At least one conductive circuit 11 below the outermost interlayer resin insulating layer and connecting with the outermost conductor portion through the via hole. The at least one conductive circuit 11 being positioned directly below the pad structure and directly on the at least one conductive circuit (see paragraph 6 and 22-33; Figs. 1, 5, and 8). Yabushita discloses the claimed invention except for the planar area of the pad structure is greater than the planar area of the conductive circuit. Applicant has not disclosed the larger pad structure solves any stated problem or is for any particular purpose. Moreover, it appears that the pad structure of Yabushita when utilized in applicant's invention, would perform equally well with the different size pad structure. Therefore, it would have been an obvious matter of design choice to have wafers having different diameters, since such a modification would have involved a mere change in the size of a component. A change is size is

generally recognized as being within the level of ordinary skill in the art. *In re Rose, 105 USPQ 237 (CCPA 1955).*

With respect to Claims 90, 104, and 125, Yabushita discloses at least one conductor layer comprising a plurality of conductor circuits 11 formed below the outermost interlayer resin insulating layer. At least one interlayer reins insulating layer formed below the conductor layer wherein the conductor layer and the interlayer resin insulating layer are alternately formed (see Fig. 4).

With respect to Claims 91-93 and 105-107, Yabushita discloses wherein the pad structure comprises an outermost conductor portion (i.e. the portion of the pad that extends above the resin insulating layer) has a outermost conductor portion that is exposed and an innermost conductor portion inner of the pad formed on the outermost interlayer resin insulating layer and the at least one conductor circuit is positioned directly below the pad structure (see Figs. 4 and 5).

With respect to Claims 94, 108, and 126, Yabushita discloses at least one lower via hole 7 directly connected to the via hole and formed through the at least one interlayer resin insulating layer formed below the conductor layer, the at least one lower via hole being configured to electrically connect the via hole to at least one of the conductor circuits in the at least one conductor layer (see paragraph 20 and 21; Figs. 1, 4, and 8).

With respect to Claims 95, 109, and 127, Yabushita discloses wherein the at least one conductor circuit is positioned directly below the pad structure (see Figs. 1 and 5).

With respect to Claims 98, 112, and 130, Yabushita discloses wherein the conductive connecting pin (i.e. conductive connecting means) comprises a columnar connection portion and a plate like secured portion, the secured portion is secured to the pad through the solder, and the conductive connecting pin comprises at least one of Cu, a copper alloy, Ti, Zn, A1 and a noble metal (see paragraph 26).

With respect to Claims 99, Yabushita discloses wherein the columnar connection portion has a constriction portion having a diameter which is smaller than a diameter of other portion (see Figs. 1, 3, and 8).

With respect to Claims 100-102, 113-115, and 131, it is inherent from Yabushita that the pad structure has a roughened surface since the pad is made of metal, which would have some level of roughness.

With respect to Claims 117, 118, 120, and 121, Yabushita discloses wherein the at least one metal layer (i.e. made of gold) formed in the partially exposed portion of the pad structure comprises at least one metal which prevents corrosion (see paragraph 26).

With respect to Claims 133 and 137, Yabushita discloses wherein the solder being disposed over at least one metal layer formed only in the partially exposed portion of the pad structure such that the solder is within the opening of the solder resist layer (see Figs. 1 and 3).

With respect to Claims 134-136 and 138, Yabushita discloses wherein the solder being disposed over at least one metal layer formed only in the partially exposed portion of the pad structure such that the solder completely covers the at least one metal layer

and contact between the solder and the at least one metal layer is entirely within the opening of the solder resist layer (see Figs. 1 and 3).

With respect to Claim 139, Yabushita discloses wherein said opening in the solder resist comprises a bottom formed by said partially exposed portion of the pad structure. A sidewall extending from the bottom in a direction of thickness of the solder resist to a planar surface of the solder resist, wherein said at least one metal layer formed only in the partially exposed portion of the pad structure consists of the at least one metal layer formed only on the bottom of the opening (see Figs. 1-3 and 5).

With respect to Claim 140, Yabushita discloses wherein said at least one metal layer comprises an edge surface extending in a direction of thickness of the at least one metal layer, wherein the edge portion touches the sidewall (see Figs. 1-3 and 5).

With respect to Claims 141 and 142, Yabushita discloses wherein the pad structure connects with a conductor circuit which is formed on a core portion of the substrate 1 (see Fig. 1).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. Claim 96, 97, 110, 111, 128, 129, and 132 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yabushita et al. (JP 08-172273) as applied to claim 1 above, and further in view of Seyama et al. (US 5,586,006).

With respect to Claims 96, 110, 128, Yabushita discloses the claimed invention except for a signal line formed on the outermost interlayer resin insulating layer, wherein the signal line electrically connects to the pad structure by circuit layers 32A. The signal line is partially covered with the solder resist. However, Seyama discloses a signal line (i.e. located attached to bump 40) formed on the outermost interlayer resin insulating layer, wherein the signal line electrically connects to the pad structure by circuit layer s 32A-2 and 32A-3. The signal line is partially covered with the solder resist (see Fig. 5). Thus, Yabushita and Seyama have substantially the same environment of a pin electrically connected to a pad of a substrate. Therefore, one skilled in the art at the time of the invention to incorporating a signal line electrically connects to the pad structure of Yabushita, since the signal line would facilitate in electrical connection between the substrate and pin as taught by Seyama.

With respect to Claim 97, 111, and 129, Yabushita discloses the claimed invention except for a diameter of the pad structure is 1.02 times to 100 times a diameter of the opening. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the a diameter of the pad structure is 1.02 times to 100 times a diameter of the opening, since it has been held that where the

general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Allen, 105 USPQ 233.*

7.

With respect to Claim 132, it is inherent from Yabushita that the pad structure has a roughened surface since the pad is made of metal, which would have some level of roughness.

12. Claims 116, 119, 122, and 123 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yabushita et al. (JP 08-172273) as applied to claims 1 and 103 above, and further in view of Hitachi (JP 10-022601).

With respect to Claims 10-14, Yabushita discloses the claimed invention except at least one metal layer formed in the partially exposed portion of the pad structure, wherein the solder is disposed over the at least one metal layer. The at least one metal layer has a plurality of layers that are formed in the partially exposed portion of the pad structure comprises at least one material selected from the group consisting of gold, silver, copper, nickel, tin, aluminum, lead, phosphorus, chrome, tungsten, molybdenum, titanium, platinum and solder. However, Hitachi discloses at least one metal layer 8 formed in the partially exposed portion of the pad structure, wherein the solder is disposed over the at least one metal layer. The at least one metal layer has a plurality of layers that are formed in the partially exposed portion of the pad structure comprises at least one material selected from the group consisting of gold, silver, copper, nickel, tin, aluminum, lead, phosphorus, chrome, tungsten, molybdenum, titanium, platinum and solder (see paragraph 5). The at least one metal layer of Hitachi would be formed in the

partially exposed portion of the pad structure of Yabushita after the opening is formed in the solder resist since the metal layer is formed of plurality of layers that in a preformed structure before attachment to the substrate. Thus, Yabushita and Hitachi has substantially the same environment of a pin electrically connected to a pad of a substrate. Therefore, one skilled in the art at the time of invention would readily recognize incorporating a plurality of metal layers on the pad structure of Yabushita, since the plurality of metal layers would facilitate the electrical connection between the substrate with an external device as taught by Hitachi.

The prior art made of record and not relied upon is cited primarily to show the product of the instant invention.

Conclusion

13. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (571) 272-1927.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system Status information for published applications may be obtained from either Private PMR or Public PMR. Status information for unpublished applications is available through Private PMR only. For more information about the PMR system see http://pair-dkect.uspto.gov. Should you

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AC/August 1, 2010

/Alonzo Chambliss/
Primary Examiner, Art Unit 2892